SESSION 21 – Honolulu Suite
Analog/RF Devices II

Thursday, June 17, 1:30 p.m.
Chairpersons: C. Bulucea, National Semiconductor
T. Dan, Sanyo Electric

21.1 — 1:30 p.m.

Engineering of Voltage Nonlinearity in High-K MIM Capacitor for Analog/Mixed-Signal ICs, S.J. Kim, B.J. Cho, M.-F. Li, S.-J. Ding, M.B. Yu*, C. Zhu, A. Chin** and D.-L. Kwong***, National University of Singapore, Singapore, *Institute of Microelectronics, Singapore, **National Chiao Tung University, Taiwan, ROC, ***University of Texas, Austin, TX

It is demonstrated for the first time that voltage linearity coefficients (VCC) of metal-insulator-metal (MIM) capacitors can be engineered and virtually zero VCC can be achieved by using high-K and SiO2 stacked dielectrics. Capacitance density of 6 fF/um2 and VCC of 14 ppm/V2 achieved in this work are the best ever reported. The HfO2/SiO2 stacked MIM shows excellent performance in other parameters as well, such as low leakage current, low TCC, and stable frequency dependence.

21.2 — 1:55 p.m.

Ultra-thin Chip with Permalloy Film for High Performance MS / RF CMOS, T. Ohguro, N. Sato, M. Matsuo, K. Kojima, H. S. Momose, K. Ishimaru and H. Ishiuchi, Toshiba Corporation Semiconductor Company, Kanagawa, Japan

In this paper, we describe the high analog performance of MOSFETs and inductors on 1.7um ultra-thin chip with permalloy film. The chip brings about a larger reduction of substrate noise and NFmin because the penetration of the noise, which passes along Psub from Nwell can be suppressed. The Q value degradation of inductor caused by the metal under thin chip can be suppressed by 10nm permalloy deposition on backside of Si substrate because the film can suppress the penetration of magnetic field into the metal.

21.3 — 2:20 p.m.

High Quality High-k MIM Capacitor by $Ta_2O_5/HfO_2/Ta_2O_5$ Multi-layered Dielectric and NH_3 Plasma Interface Treatments for Mixed-Signal/RF Applications, Y.-K. Jeong, S.-J. Won, D.-J. Kwon, M.-W. Song, W.-H. Kim, M.-H. Park, J.-H. Jeong, H.-S. Oh, H.-K. Kang and K.-P. Suh, Samsung Electronics Co., Ltd., Kyungki-Do, Korea

Novel high-k MIM capacitor technology for mixed-signal/RF applications has been successfully developed by introducing multi-layered high-k dielectric(Ta2O5/HfO2/Ta2O5) and NH3 plasma electrode-dielectric interfaces treatments. For the first time, we have simultaneously achieved high capacitance of 4fF/um2 and low leakage current of 100nA/cm2 at high temperature of 125oC with ultra low VCC(a=16.9ppm/V2, b=5.2ppm/V) and high Q(~107 at 2.4GHzand 5.4pF).

21.4 — 2:45 p.m.

A Comparison of State-of-the-Art NMOS and SiGe HBT Devices for Analog/Mixed-signal/RF Circuit Applications, K. Kuhn, R. Basco, D. Becher, M. Hattendorf, P. Packan, I. Post, P. Vandervoorn and I.Young, Intel Corporation, Hillsboro, OR

RF CMOS performance from a 90nm derivative communications process technology is compared to SiGe BJT performance. NMOS performance at fT/fmax = 209/248 GHz(70nm) and fT/fmax = 166/277 GHz (80nm) with Fmin at 0.3 dB (2GHz) and 0.6 dB(10GHz) suggests there is no major reason to implement SiGe HBTs BiCMOS in an integrated communications process.